

IEEE Standard for System, Software, and Hardware Verification and Validation

IEEE Computer Society

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Software and Systems Engineering Standards Committee

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IEEE Std 1012™-2016
(Revision of
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Abstract: Verification and validation (V&V) processes are used to determine whether the development products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. V&V life cycle process requirements are specified for different integrity levels. The scope of V&V processes encompasses systems, software, and hardware, and it includes their interfaces. This standard applies to systems, software, and hardware being developed, maintained, or reused (legacy, commercial off-the-shelf [COTS], non-developmental items). The term *software* also includes firmware and microcode, and each of the terms *system*, *software*, and *hardware* includes documentation. V&V processes include the analysis, evaluation, review, inspection, assessment, and testing of products.

Keywords: acceptance testing, architecture evaluation, component testing, concept documentation evaluation, criticality, criticality analysis, design evaluation, disposal plan evaluation, environmental verification and validation (V&V) factors, hardware life cycle, hardware V&V, hardware verification and validation, hazard analysis, IEEE 1012, implementation evaluation, independent verification and validation (IV&V), integration testing, integrity level, interface analysis, IV&V, minimum V&V tasks, nth of a kind, objective evidence, operating procedure evaluation, qualification testing, quality assurance, regression analysis, regression testing, requirements allocation analysis, requirements evaluation, reuse software, risk analysis, security analysis, software life cycle, software quality assurance (SQA), software V&V, software verification and validation, source code documentation evaluation, source code evaluation, SQA, stakeholder needs and requirements evaluation, system element interaction analysis, system life cycle, system maintenance strategy assessment, system of interest, system requirements evaluation, system V&V, system verification and validation, testing, traceability analysis, V&V, V&V measures, validation, verification

The Institute of Electrical and Electronics Engineers, Inc.
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Rosnyev Alvarado
Steven Baird, Jr.
Arde Bedjanian
Luis Betancourt
Susan M. Burgess
Tiffany Burgess
William Burgess
Norbert Carte
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Jiayu Chen
Larry Chi
Ivan Chow
Pong C. Chung
Darrell Cooksey
Ken Costello

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Harpal Dhama
Ronald F. Dean, Sr.
Jun Ding
Stephen Driskell
Eva Freund
Jon D. Hagar
Libing He
YanJun He
John W. Hefler
David Hooten
George R. Hughes
Yu-chih Ko
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Lingpo Li
Gang Ma

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Robert R. Moniri
Owen Nelson
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Scott W. Schield
Raymond R. Senechal
Li Shi
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Murat S. Uzman
Yichun Wu
Steve Yang
Xiaobai Yu

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

Edward A. Addy
Robert Aiello
Johann Amsenga
T. Scott Ankrum
Lee Armstrong
Steven Baird, Jr.
Bakul Banerjee
Pieter Botman
Susan M. Burgess
Juan Carreon
Sue Carroll
Keith Chow
Raul Colcher
Paul Croll
Geoffrey Darnton
Ronald F. Dean, Sr.
Grazia D'Elia
Harpal Dhama
Teresa Doran
Sourav Dutta
Andrew Fieldsend
Eva Freund
David Friscia
Roger U. Fujii
David Fuschi
Gregg Giesler
Randall Groves

Jon D. Hagar
John Harauz
David Herrell
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Bernard Homes
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Don Wright
Yu Yuan
Daidi Zhong

*Member Emeritus

Participants

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The following members of the individual balloting committee voted on Corrigendum 1 of this standard. Balloters may have voted for approval, disapproval, or abstention.

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Johann Amsenga
Steven Baird, Jr.
Ulas Baloglu
Patti Brideson
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Introduction

This introduction is not part of IEEE Std 1012™-2016, IEEE Standard for System, Software, and Hardware Verification and Validation.

The Verification and Validation processes are technical processes of systems, software, and hardware engineering. The Verification process and the Validation process are interrelated and complementary processes, and are referenced together as *verification and validation (V&V)*. The purpose of V&V is to help the organization build quality into the system during the life cycle. V&V processes provide an objective assessment of products and processes throughout the life cycle. This assessment demonstrates whether the requirements are correct, complete, accurate, consistent, and testable. The V&V processes determine whether the development products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. The determination includes the assessment, analysis, evaluation, review, inspection, and testing of products and processes. V&V is performed in parallel with all life cycle stages, not at their conclusion.

V&V is an extension of program management and systems, software, and hardware engineering that employs a rigorous methodology to identify objective data and conclusions to provide feedback about quality, performance, and schedule to the supplier. This feedback consists of anomaly resolutions, performance improvements, and quality improvements not only for expected operating conditions but also across the full spectrum of the system and its interfaces. Early feedback results allow the organization to modify the products in a timely fashion and thereby reduce overall project and schedule impacts. Without a proactive approach, the anomalies and associated system changes are typically delayed to later in the program schedule, resulting in greater program costs and schedule delays.

IEEE Std 1012 is a process standard that defines the V&V processes in terms of specific activities and related tasks. The standard also defines the contents of the V&V plan (VVP), including example formats.

V&V may be performed at the level of the system, software element, or hardware element, or on any combination of these. V&V may also be performed on an element of a system, including a subordinate system (i.e., subsystem). Throughout this standard, the term *hardware* means an electronic or mechanical hardware element. In each case, the V&V processes are invoked, either in parallel or recursively, across the full life cycle of the system or element.

This version of the standard is a revision to IEEE Std 1012-2012 [B5].¹ The earliest version of this standard (1986) described the content of a software V&V plan, with subsequent versions (1998 and 2004) changing the focus from the software V&V plan to software V&V processes. The 2012 revision expanded the scope of the V&V processes to include systems and hardware as well as software. This revision aligns more completely with the terminology and structure of ISO/IEC/IEEE 15288:2015(E) [B16] and ISO/IEC 12207:2008 [B11]. The following is a summary of the changes made in this version:

- No new V&V activities or tasks have been added other than to address the new or modified processes from ISO/IEC/IEEE 15288:2015(E) [B16], and conformance to this standard can be readily aligned with conformance to the V&V clauses of ISO/IEC/IEEE 15288. Some V&V activities and tasks have been rearranged to facilitate understanding and ease of use.
- The terminology, structure, and mappings were revised to be consistent with ISO/IEC/IEEE 15288:2015(E) [B16].

The following key concepts are emphasized in this standard:

- Integrity levels. Defines four integrity levels to describe the importance of the system, software, and hardware, varying from high integrity to low integrity, to the user.

¹ The numbers in brackets correspond to those of the bibliography in [Annex N](#).

- Minimum V&V tasks for each integrity level. Defines the minimum V&V tasks required for each of the four integrity levels.
- Optional V&V tasks. Includes a table of optional V&V tasks for tailoring the V&V effort to address the project needs and application-specific characteristics.
- Intensity and rigor applied to V&V tasks. Includes the concept that the intensity and rigor applied to the V&V tasks vary according to the integrity level. Higher integrity levels require the application of greater intensity and rigor to the V&V task. Intensity includes a greater scope of analysis across all normal and abnormal system operating conditions. Rigor includes more formal techniques and recording procedures.
- Detailed criteria for V&V tasks. Defines specific criteria for each V&V task, including minimum criteria for correctness, consistency, completeness, accuracy, readability, and testability. The V&V task descriptions include a list of the required task inputs and outputs.
- Systems viewpoints. Includes minimum software and hardware V&V tasks to address system issues. These tasks include hazard analysis, security analysis, risk analysis, migration assessment, and retirement assessment. Specific system issues are contained in individual V&V task criteria.
- Conformance to international and IEEE standards. Defines the V&V processes to conform to life cycle process standards such as ISO/IEC/IEEE 15288:2015(E) [\[B16\]](#) and ISO/IEC 12207:2008 [\[B11\]](#), as well as the entire family of IEEE software engineering standards. This standard addresses all system and software life cycle processes, including the Agreement, Organizational Project-Enabling, Project, Technical, Software Implementation, Software Support, and Software Reuse process groups. This standard is compatible with all life cycle models; however, not all life cycle models use all of the life cycle processes described in this standard.

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IEEE Standard for System, Software, and Hardware Verification and Validation

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1. Overview

1.1 Scope

This verification and validation (V&V) standard is a process standard that addresses all system, software, and hardware life cycle processes including the Agreement, Organizational Project-Enabling, Project, Technical, Software Implementation, Software Support, and Software Reuse process groups. This standard is compatible with all life cycle models (e.g., system, software, and hardware); however, not all life cycle models use all of the processes listed in this standard.

V&V processes determine whether the development products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. This determination may include the analysis, evaluation, review, inspection, assessment, and testing of products and processes.

The user of this standard may invoke those life cycle processes and the associated V&V processes that apply to the project. A description of system life cycle processes may be found in ISO/IEC/IEEE 15288:2015(E) [B16],¹ and a description of software life cycle processes may be found in ISO/IEC 12207:2008 [B11]. Annex A maps ISO/IEC/IEEE 15288:2015(E) [B16] (Table A.1 and Table A.2) and ISO/IEC 12207:2008 [B11] (Table A.3 and Table A.4) to the V&V activities and tasks defined in this standard.

This standard defines the verification and validation processes that are applied to the system, software, and hardware development throughout the life cycle, including acquisition, supply, development, operations,

¹ The numbers in brackets correspond to those of the bibliography in Annex N.

maintenance, and retirement. This standard applies to the system, software, and hardware being acquired, developed, maintained, or reused. The term *software* also includes firmware and microcode (e.g., Field Programmable Gate Arrays and Programmable Logic Devices). Each of the terms *system*, *software*, and *hardware* includes its associated documentation.

V&V processes consist of the Verification process and the Validation process. The Verification process provides objective evidence for whether the products:

- Conform to requirements (e.g., for correctness, completeness, consistency, and accuracy) for all activities during each life cycle process.
- Satisfy the standards, practices, and conventions during life cycle processes.
- Successfully complete each life cycle activity and satisfy all the criteria for initiating succeeding life cycle activities (i.e., builds the product correctly).

The Validation process provides evidence for whether the products:

- Satisfy system requirements allocated to the products at the end of each life cycle activity.
- Solve the right problem (e.g., correctly model physical laws, implement business rules, and use the proper system assumptions).
- Satisfy intended use and user needs in the operational environment (i.e., builds the correct product).

The Verification process and the Validation process are interrelated and complementary processes that use each other's process results to establish better completion criteria and analysis, evaluation, review, inspection, assessment, and test V&V tasks for each life cycle activity. The V&V task criteria described in [Table 1a](#) through [Table 1d](#) explicitly define the conformance requirements for V&V processes.

The development of a sufficient body of evidence requires a trade-off between the amount of time spent and a finite set of system conditions and assumptions against which to perform the V&V tasks. Each project should define criteria for a sufficient body of evidence (e.g., selecting an integrity level), the schedule, and the scope of the V&V analysis and test tasks.

This standard does not assign the responsibility for performing the V&V tasks to any specific organization. The analysis, evaluation, and test activities may be performed by multiple organizations; however, the methods and purpose will differ for each organization's functional objectives.

ISO/IEC/IEEE 15288:2015(E) [\[B16\]](#) includes tasks for the supplier to execute the agreement according to established project plans and to deliver the product or service in accordance with the agreement criteria. The techniques described in this standard are useful in performing the supplier's tests and evaluations. Therefore, whenever this standard mentions the supplier's performance of a verification or validation activity, it is to be understood that the reference applies to the test and evaluation tasks of system development.

1.2 Purpose

The purpose of this standard is to:

- Establish a common framework of the V&V processes, activities, and tasks in support of all system, software, and hardware life cycle processes.
- Define the V&V tasks, required inputs, and required outputs in each life cycle process.
- Identify the minimum V&V tasks corresponding to a four-level integrity schema.
- Define the content of the Verification and Validation Plan.