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IEEE Standard for System and Software Verification and Validation

IEEE Computer Society

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Software & Systems Engineering Standards Committee (C/S2ESC)

IEEE
3 Park Avenue
New York, NY 10016-5997
USA

25 May 2012

IEEE Std 1012™-2012
(Revision of
IEEE Std 1012-2004)

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Approved 29 March 2012

IEEE-SA Standards Board

Abstract: Verification and validation (V&V) processes are used to determine whether the development products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. V&V life cycle process requirements are specified for different integrity levels. The scope of V&V processes encompasses systems, software, and hardware, and it includes their interfaces. This standard applies to systems, software, and hardware being developed, maintained, or reused [legacy, commercial off-the-shelf (COTS), nondevelopmental items]. The term *software* also includes firmware and microcode, and each of the terms *system*, *software*, and *hardware* includes documentation. V&V processes include the analysis, evaluation, review, inspection, assessment, and testing of products.

Keywords: environmental verification and validation (V&V) factors, hardware V&V, IEEE 1012, integrity level, independent V&V (IV&V), risk/hazard/security analyses, software life cycle, software V&V, system life cycle, system V&V, V&V, V&V measures, V&V of reuse software

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PDF: ISBN 978-0-7381-7268-2 STD97243
Print: ISBN 978-0-7381-7374-0 STDPD97243

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Introduction

This introduction is not part of IEEE Std 1012-2012, IEEE Standard for System and Software Verification and Validation.

Verification and validation (V&V) is a technical discipline of systems engineering. The purpose of V&V is to help the development organization build quality into the system during the life cycle. V&V processes provide an objective assessment of products and processes throughout the life cycle. This assessment demonstrates whether the requirements are correct, complete, accurate, consistent, and testable. The V&V processes determine whether the development products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. The determination includes the assessment, analysis, evaluation, review, inspection, and testing of products and processes. V&V is performed in parallel with all life cycle stages, not at their conclusion.

V&V is an extension of program management and systems engineering that employs a rigorous methodology to identify objective data and conclusions to provide feedback about quality, performance, and schedule to the supplier. This feedback consists of anomaly resolutions, performance improvements, and quality improvements not only for expected operating conditions but also across the full spectrum of the system and its interfaces. Early feedback results allow the development organization to modify the products in a timely fashion and thereby reduce overall project and schedule impacts. Without a proactive approach, the anomalies and associated system changes are typically delayed to later in the program schedule, resulting in greater program costs and schedule delays.

IEEE Std 1012™-2012 is a process standard that defines the V&V processes in terms of specific activities and related tasks. The standard also defines the contents of the V&V plan (VVP), including example formats.

V&V may be performed at the level of the system, software element, or hardware element, or on any combination of these. V&V may also be performed on an element of a system, including a subordinate system (i.e., subsystem). Throughout this standard, the term *hardware* means an electronic or mechanical hardware element. In each case, the V&V processes are invoked, either in parallel or recursively, across the full life cycle of the system or element.

This version of the standard is a major revision to IEEE Std 1012™-2004 [B5].[a] The earliest version of this standard (1986) described the content of a software V&V plan, with subsequent versions (1998 and 2004) changing the focus from the software V&V plan to software V&V processes. This revision expands the scope of the V&V processes to include systems and hardware as well as software. It also aligns the terminology and structure to be consistent with ISO/IEC 15288:2008 [B16] and ISO/IEC 12207:2008 [B11]. The following is a summary of the changes made in this version:

a) No new software V&V activities or tasks have been added, and the use of IEEE Std 1012-2004 [B5] is compliant with the software V&V clauses of this standard. Some software V&V activities and tasks have been rearranged to facilitate the understanding and ease of use.
b) System V&V activities and tasks and hardware V&V activities and tasks were added to the existing software V&V standard.
c) The standard was restructured to allow for the performance of system, software, and hardware V&V individually or in any combination. The standard contains separate clauses that address common, system, software, and hardware V&V activities.
d) The terminology, structure, and mappings were revised to be consistent with ISO/IEC 12207:2008 [B11]. The new system V&V terminology, structure, and mappings are consistent with ISO/IEC 15288:2008 [B16].

[a] The numbers in brackets correspond to those of the bibliography in Annex M.

The following key concepts are emphasized in this standard:

- *Integrity levels.* Defines four integrity levels to describe the importance of the system, software, and hardware, varying from high integrity to low integrity, to the user.
- *Minimum V&V tasks for each integrity level.* Defines the minimum V&V tasks required for each of the four integrity levels. Includes a table of optional V&V tasks for tailoring the V&V effort to address the project needs and application-specific characteristics.
- *Intensity and rigor applied to V&V tasks.* Includes the concept that the intensity and rigor applied to the V&V tasks vary according to the integrity level. Higher integrity levels require the application of greater intensity and rigor to the V&V task. Intensity includes a greater scope of analysis across all normal and abnormal system operating conditions. Rigor includes more formal techniques and recording procedures.
- *Detailed criteria for V&V tasks.* Defines specific criteria for each V&V task, including minimum criteria for correctness, consistency, completeness, accuracy, readability, and testability. The V&V task descriptions include a list of the required task inputs and outputs.
- *Systems viewpoints.* Includes minimum software and hardware V&V tasks to address system issues. These tasks include hazard analysis, security analysis, risk analysis, migration assessment, and retirement assessment. Specific system issues are contained in individual V&V task criteria.
- *Conformance to international and IEEE standards.* Defines the V&V processes to conform to life cycle process standards such as ISO/IEC 15288:2008 [B16], IEEE Std 1074™-2006 [B9], and ISO/IEC 12207:2008 [B11], as well as the entire family of IEEE software engineering standards. This standard addresses all system and software life cycle processes, including the Agreement, Organizational Project-Enabling, Project, Technical, Software Implementation, Software Support, and Software Reuse process groups. This standard is compatible with all life cycle models; however, not all life cycle models use all of the life cycle processes described in this standard.

Contents

IEEE Standard for System and Software Verification and Validation

1. Overview

1.1 Scope

This verification and validation (V&V) standard is a process standard that addresses all system and software life cycle processes including the Agreement, Organizational Project-Enabling, Project, Technical, Software Implementation, Software Support, and Software Reuse process groups. This standard is compatible with all life cycle models (e.g., system, software, and hardware); however, not all life cycle models use all of the processes listed in this standard.

V&V processes determine whether the development products of a given activity conform to the requirements of that activity and whether the product satisfies its intended use and user needs. This determination may include the analysis, evaluation, review, inspection, assessment, and testing of products and processes.

The user of this standard may invoke those life cycle processes and the associated V&V processes that apply to the project. A description of system life cycle processes may be found in ISO/IEC 15288:2008 [B16],[1] and a description of software life cycle processes may be found in ISO/IEC 12207:2008 [B11] and IEEE Std 1074™-2006 [B9]. Annex A maps ISO/IEC 15288:2008(E) [B16] (Table A.1 and Table A.2) and ISO/IEC 12207:2008 [B11] (Table A.3 and Table A.4) to the V&V activities and tasks defined in this standard.

[1] The numbers in brackets correspond to those of the bibliography in Annex M.